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10EC56

Fifth Semester B.E. Degree Examination, Dec.2016/Jan.2017
Fundamentals of CMOS VLSI

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the action of enhancement mode transistor for different values of V_{gs} and V_{ds}. **(08 Marks)**

b. Explain the second order effects viz.
(i) Focoler Nordheium Tunneling.
(ii) Drain punch through.
(iii) Impact ionization. **(06 Marks)**

c. Describe in detail CMOS fabrication in an P-well process. **(06 Marks)**

2 a. Draw schematic, stick diagram, layout for nMOS 2-input NOR gate, where 4 : 1 ratio for pull up and 1 : 1 ratio for each pull-down. Specify λ-based rules for layout. **(12 Marks)**

b. Provide the λ-based design rules for transistors, contact cuts and vias. **(08 Marks)**

3 a. Realize 2-input NAND gate as example in,
(i) BiCMOS logic.
(ii) Pseudo-nMOS logic.
Discuss merits and demerits. **(10 Marks)**

b. Explain the dynamic CMOS logic with example. List the problems and solution for issues. **(10 Marks)**

4 a. What are the scaling factor for:
(i) Gate capacitance
(ii) Maximum operating frequency
(iii) Current density
(iv) Power speed product. **(10 Marks)**

b. Define sheet resistance and standard unit of capacitance □Cg. Calculate the ON resistance for NMOS inverter with R_{SN} = 10 KΩ, $Z_{PU} = 4$ and $Z_{pd} = 1$, V = 5 V. And calculate power dissipiation. **(10 Marks)**

PART – B

5 a. Design a parity generator, where output is 1 for even number of one's and draw the stick diagram for one basic cell. **(10 Marks)**

b. In the circuit shown in Fig. Q5 (b). Find V_1, V_2, V_3, V_4. Assume threshold voltage of each transistor is V_{tn}. **(04 Marks)**

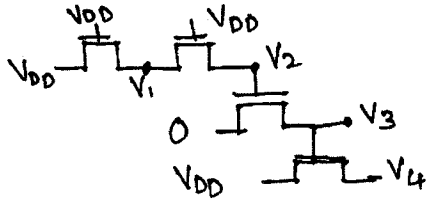

Fig. Q5 (b)

c. Draw the basic form of a 2-ϕ clock generator and explain. **(06 Marks)**

6 a. Discuss the architectural issues to be followed in the design of a VLSI sub-system. **(06 Marks)**
b. Realize a 4×4 barrel shifter using MOS switches and explain in brief. **(06 Marks)**
c. Explain carry skip adder. **(08 Marks)**

7 a. Discuss the various system timing consideration. **(04 Marks)**
b. Explain the 3T DRAM cell with stick diagram. **(10 Marks)**
c. Describe the CMOS pseudo-static RAM circuit. **(06 Marks)**

8 a. Explain different types of Input/Output pads. **(05 Marks)**
b. List the ground rules for a system design. **(05 Marks)**
c. Write a note on Built-in self test. **(05 Marks)**
d. Write a note on BiCMOS logic with neat circuit. **(05 Marks)**

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